TECHNICAL DATA

MOTOROLA HEP®

INTEGRATED CIRCUITS

INCLUDING BOTH DIGITAL AND LINEAR DEVICES

This brochure contains all of the data, specifications, and electrical characteristics of the Integrated Circuits that are included in the Motorola HEP line of semi-conductors. These devices have been carefully selected from the very extensive Motorola line of IC's in an effort to offer the serious Hobbyist, Experimenter, Professional, as well as the student, with economical and quality units that will enable them to design, construct, and utilize IC projects to the fullest extent.

Three distinct IC families are offered in the HEP line, i.e. ECL (Emitter Coupled Logic) which features extremely fast switching and low power consumption; RTL (Resistor Transistor Logic), which is slower but very dependable, easy to work with, and widely used; and Linear for audio, RF, IF, and agc applications.

ECL
- HEP553 Half Adder
- HEP554 Bias Driver
- HEP556 3-Input Gate
- HEP558 J-K Flip-Flop

RTL
- HEP570 Quad 2-Input Gate
- HEP571 Dual Buffer
- HEP572 Dual J-K Flip-Flop
- HEP580 Dual 2-Input Gate
- HEP581 4-Input Gate
- HEP582 Dual Buffer
- HEP583 J-K Flip-Flop
- HEP584 Dual 2-Input Gate
- HEK-1 Integrated Circuit Kit
  (Contains 2 HEP580, 1 HEP581, 1 HEP582, 1 HEP583)

LINEAR
- HEP590 High Frequency Amplifier
- HEP591 Wide Band Amplifier/Discriminator
- HEP592 Stereo Preamplifier
- HEP593 Audio Power Amplifier

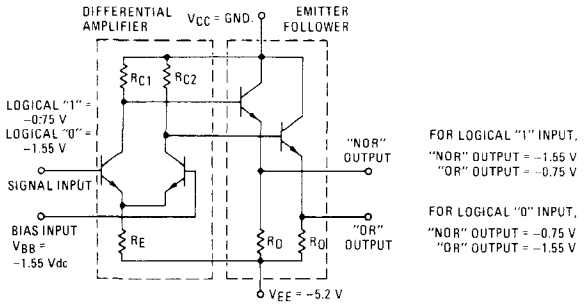
MOTOROLA Semiconductor Products Inc.

GENERAL ECL INFORMATION

The ECL line of IC's was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical ECL circuit comprises a differential-amplifier input, with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter-followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

BASIC ECL GATE CIRCUIT



POWER SUPPLY CONNECTIONS Any one of the power supply nodes, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the manufacturer has found it most convenient to ground the V_{CC} node. In such a case: V_{CC} = 0, V_{BB} = −1.15 V, V_{EE} = 5.2 V.

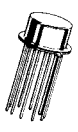
SYSTEM LOGIC SPECIFICATIONS The output logic swing of 0.8 V then varies from V_L = −1.55 V to V_H = −0.75 V with respect to ground. Positive logic is used when reference is made to logical "0's" or "1's". Then "0" = −1.55 V; "1" = −0.75, typical. Dynamic logic refers to a change of logic states. Dynamic "0" is a negative going voltage excursion and a dynamic "1" is a positive going voltage excursion.

CIRCUIT OPERATION A fixed bias of −1.15 volts is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logic "0" is applied, the current through R_E is supplied by the fixed-biased transistor. A drop of 800 mV occurs across R_{C2}. The OR output then is −1.55 V, or one V_{BE} drop below 800 mV. Since no current flows in the "signal input" transistor, the NOR output is a V_{BE} drop below ground, or −0.75 volts. When a logical "1" level is applied to the "signal input", the current through R_{C2} is switched to the "signal input" transistor and a drop of 800 mV occurs across R_{C1}. The OR output then goes to −0.75 volts and the NOR output goes to −1.55. Note: Any unused input should be connected to V_{EE}.

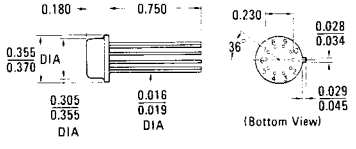
BIAS VOLTAGE SOURCE A fixed-bias voltage applied to the bias input is obtained from a regulated, temperature-compensated bias driver, HEP554. The temperature characteristics of the bias driver compensate for any variations in circuit operating point over the temperature range or supply voltage changes, to insure that the threshold point is always in the center of the transition region. The bias driver can be used to drive up to 25 logic elements and should be employed for all elements except those with built-in bias networks.

PACKAGING All HEP ECL integrated circuits are packaged in the Motorola case type 71 metal packages.

10 LEAD METAL PACKAGE



Case 71 (Modified TO-5)



All types – Pin 2 connected to case

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-10	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 Vdc to V_{EE}	Vdc
Output Source Current	I_O	20	mAdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	+15 to +55	°C
AC Fan-In (Expandable Gates)	m	18	–
AC Fan-Out* (Gates and Flip-Flops)	n	15	–

*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

DEFINITIONS

e_{in} AC signal applied to the input

I_C Amount of current drawn from the positive power supply by the test unit

I_E Amount of current drawn from the test unit by the negative power supply

I_{in} Current drawn by the input of the test unit when a logical "1" (V_H) is applied to the input

I_L Current drawn from a node when that node is at ground potential

t_{d1} Time required for the output pulse to reach the 50% point of its leading edge when referenced to the 50% point of the input pulse leading edge

t_{d2} Time required for the output pulse to reach the 50% point of its trailing edge when referenced to the 50% point of the input pulse trailing edge

t_{df} Time required for a flip-flop output to reach the 50% point of its negative going edge when referenced to the 50% point of the input pulse leading edge

t_{dr} Time required for a flip-flop output to reach the 50% point of its positive going edge when referenced to the 50% point of the input pulse leading edge

t_f Time required for the output pulse to go more negative from its 90% point to its 10% point

t_r Time required for the output pulse to go more positive from its 10% point to its 90% point

V_1 "NOR" output voltage – logical "1" level output voltage when a logical "0" level (V_L) is applied to the input

V_2 "OR" output voltage – logical "0" level output voltage when a logical "0" level (V_L) is applied to the input

V_3 Saturation breakpoint voltage which corresponds to the "NOR" output characteristic where the rate of change in the output voltage to the rate of change in input voltage is zero

V_4 "NOR" output voltage – logical "0" level output voltage when a logical "1" level ($V_{1\ max}$) level is applied to the input

V_5 "OR" output voltage – logical "1" level output voltage when a logical "1" ($V_{1\ max}$) level is applied to the input

V_6 Output latch voltage – input voltage to a flip-flop which causes the output voltage to change from a logical "1" level to a logical "0" level and corresponds to the point where the rate of change in the output voltage to the rate of the input voltage approaches infinity

V_H Logical "1" input voltage

V_L Logical "0" input voltage

$\triangle V_1$ Change in the "1" level output voltage as the load is

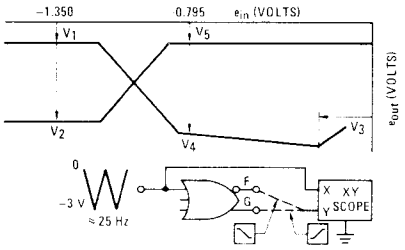
$\triangle V_5$ varied from no load to full load

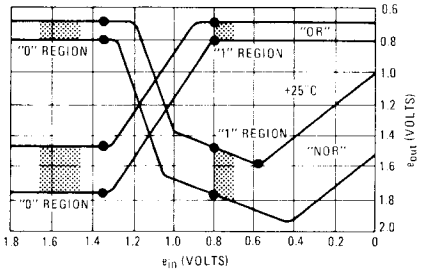
GENERAL ECL INFORMATION (Continued)

WORST-CASE TRANSFER CHARACTERISTICS

The following graphs show minimum and maximum limits of major parameters associated with the transfer characteristics of the ECL line. Min-Max limits, given at 25°C can be interpreted for design purposes as 10% to 90% spreads at all points on the curve except for guaranteed points in the Electrical Characteristics tables.

DEFINITIONS

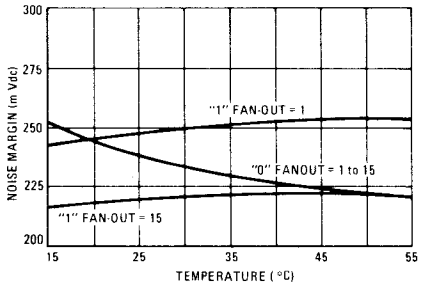




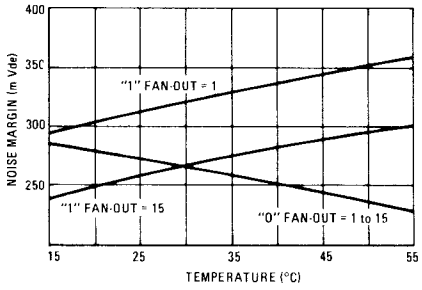
NOISE MARGINS (90 PERCENTILE)

The following graphs show worst-case Noise Margins as a function of temperature and fan-out. Top graph illustrates the advantage gained through use of HEP554 bias driver, as compared with non-compensated fixed bias source, bottom. Note: Any unused input should be connected to V_{EE}.

USING HEP 554



USING FIXED V_{BB} OF −1.15 VOLTS



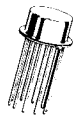
HEP 554 — ECL BIAS DRIVER

Circuit Operation: The divider network R_1, R_2, D_1, D_2, compensates for temperature variations of the base-emitter voltages of Q_1 and of the driven gates, producing a bias voltage for the ECL logic circuits that maintains a constant set of dc operating conditions over the temperature range of 0 to +75 C. In addition, compensation for power supply variations is achieved, since the bias output voltage is derived from the system supply.

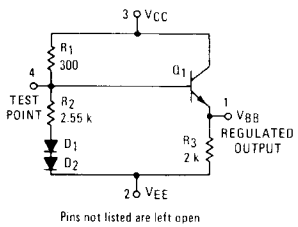
Either of the supply voltage nodes may be used as ground, however the ground potential of the bias driver must coincide with that of the logic system. Thus, if V_{CC} is grounded in the logic system, then —

V_{CC} = +6.0V V_{EE} = 0

V_{BB} = +4.8V nominal output voltage at 25°C



Case 71



Pins not listed are left open

ELECTRICAL CHARACTERISTICS

@ Test Temperature +25°C		Test Conditions Vdc ± 1%				Symbol	Test Limits +25°C		Unit
Characteristic		V_{EE} Pin No	I_L Pin No	Ground Pin No		Pin No in ( )	Min	Max	
Power Supply Drain Current		2	–	3		I_E (2)	–	4.4	mAdc
Output Voltage		2	1①	3		V_{BB}	−1.09	−1.22	Vdc

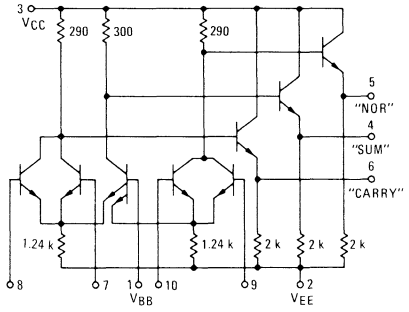
Pins not listed are left open.

①Current test conditions; no load = 0; full load = −2.5 mAdc ±5%.

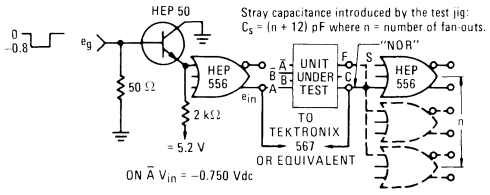
HEP 553 – ECL HALF ADDER

Half-adder that provides the "SUM", "CARRY", and "NOR" functions simultaneously.

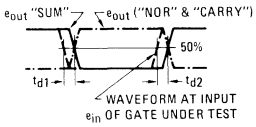
Case 71



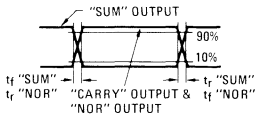
SWITCHING TIME TEST CIRCUIT



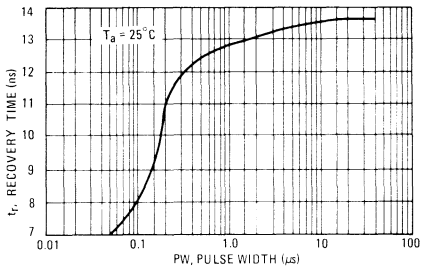
PROPAGATION DELAY

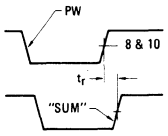


RISE & FALL TIMES



RECOVERY CHARACTERISTICS WITH SIMULTANEOUS "0" ON ALL INPUTS

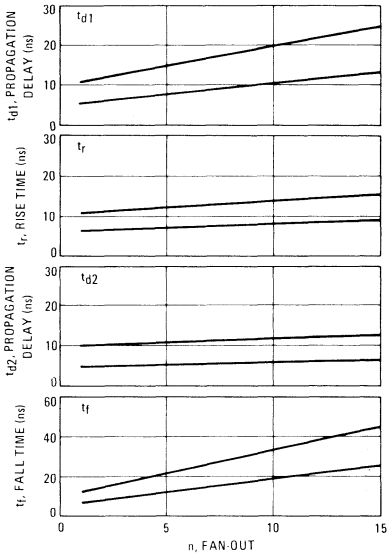




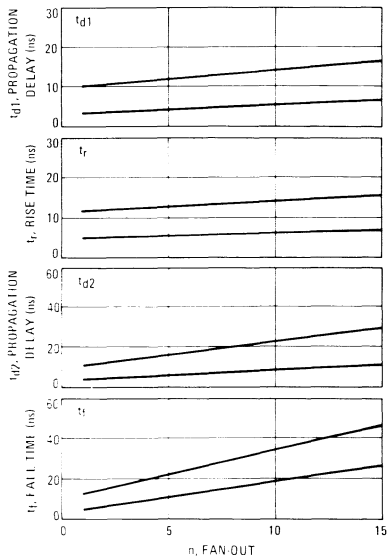
PINS 7 & 9 ARE LOGICAL "0"
PINS 8 & 10 ARE TIED TOGETHER
TO PULSE GENERATOR OUTPUT

SWITCHING CHARACTERISTICS (10% TO 90% DISTRIBUTION @ 25°C)

"SUM"



"NOR" and "CARRY"



HEP 553 – ECL HALF ADDER (Continued)

ELECTRICAL CHARACTERISTICS

@ Test Temperature +25°C	Test Conditions Vdc ± 1%									Test Limits +25°C		
	−0.670	−0.795	−1.350	−5.20	−1.15							
Characteristic	V_H Pin No	V_l max Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Min	Max	Unit
Power Supply Drain Current	–	–	–	2,7,8,9,10	1	–	–	3	I_E (2)	–	15.3	mAdc
Input Current	7	–	–	2,8,9,10	1	–	–	3	I_{in} (7)	–	100	μAdc
	8	–	–	2,7,9,10	1	–	–	3	I_{in} (8)	–	↓	↓
	9	–	–	2,7,8,10	1	–	–	3	I_{in} (9)	–		
	10	–	–	2,7,8,9	1	–	–	3	I_{in} (10)	–		
"NOR" Logical "1"	–	–	9	2,7,8,10	1	–	–	3	V_l (5)	−0.670	−0.795	Vdc
Output Voltage	–	–	10	2,7,8,9	1	–	–	3	V_l (5)	−0.670	−0.795	Vdc
"NOR" Logical "0"	–	9	–	2,7,8,10	1	–	–	3	V_4 (5)	−1.465	−1.750	Vdc
Output Voltage	–	10	–	2,7,8,9	1	–	–	3	V_4 (5)	−1.465	−1.750	Vdc
"CARRY" Logical "1"	–	–	7	2,8,9,10	1	–	–	3	V_l (6)	−0.670	−0.795	Vdc
Output Voltage	–	–	8	2,7,9,10	1	–	–	3	V_l (6)	−0.670	−0.795	Vdc
"CARRY" Logical "0"	–	7	–	2,8,9,10	1	–	–	3	V_4 (6)	−1.465	−1.750	Vdc
Output Voltage	–	8	–	2,7,9,10	1	–	–	3	V_4 (6)	−1.465	−1.750	Vdc
"SUM" Logical "1"	–	7,9	–	2,8,10	1	–	–	3	V_5 (4)	−0.670	−0.795	Vdc
Output Voltage	–	8,10	–	2,7,9	1	–	–	3	V_5 (4)	−0.670	−0.795	Vdc
"SUM" Logical "0"	–	7	10	2,8,9	1	–	–	3	V_2 (4)	−1.465	−1.750	Vdc
Output Voltage	–	8	10	2,7,9	1	–	–	3	V_2 (4)	↓	↓	↓
	–	9	8	2,7,10	1	–	–	3	V_2 (4)			
	–	10	7	2,8,9	1	–	–	3	V_2 (4)			
"NOR" Output Voltage Change (No load to full load)	–	10	–	2,7,8,9	1	–	5 ②	3	$\triangle V_l$ (5)	–	0.055	Volts
"CARRY" Output Voltage Change (No load to full load)	–	–	7	2,8,9,10	1	–	6 ②	3	$\triangle V_l$ (6)	–	0.055	Volts
"SUM" Output Voltage Change (No load to full load)	–	7,10	–	2,8,9	1	–	4 ②	3	$\triangle V_5$ (4)	–	0.055	Volts
"NOR" Saturation Breakpoint Voltage	–	–	–	2,7,8,9	1	10 ①	–	3	V_3 (5)	–	0.550	Vdc
"CARRY" Saturation Breakpoint Voltage	–	–	–	2,8,9,10	1	7 ①	–	3	V_3 (6)	–	0.550	Vdc
Switching Times						Pulse In	Pulse Out			Typ	Max	
Propagation Delay Time	–	–	–	2,7,8,9	1	10	5	3	t_{dl} (5)	6.5	11.0	ns
	–	–	–	2,8,9,10	1	7	6	3	t_{dl} (6)	6.5	11.0	↓
	–	7	–	2,8,9	1	10	4	3	t_{dl} (4)	6.5	11.5	
	–	–	–	2,7,8,9	1	10	5	3	t_{d2} (5)	8.5	13.5	
	–	–	–	2,8,9,10	1	7	6	3	t_{d2} (6)	8.5	13.5	
	–	7	–	2,8,9	1	10	4	3	t_{d2} (4)	6.0	11.0	
Rise Time	–	–	–	2,7,8,9	1	10	5	3	t_r (5)	9.0	12.5	
	–	–	–	2,8,9,10	1	7	6	3	t_r (6)	9.0	12.5	
	–	7	–	2,8,9	1	10	4	3	t_r (4)	7.0	11.5	
Fall Time	–	–	–	2,7,8,9	1	10	5	3	t_f (5)	9.5	14.0	
	–	–	–	2,8,9,10	1	7	6	3	t_f (6)	9.5	14.0	
	–	7	–	2,8,9	1	10	4	3	t_f (4)	9.5	14.0	

Pins not listed are left open.

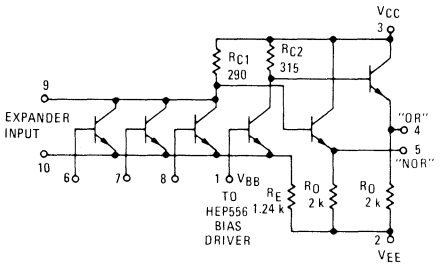
① Input voltage is adjusted to obtain dv"NOR"/dV_{in} = 0 or dV "CARRY"/dV_{in} = 0.

② Current test conditions: no load = 0; full load = −2.5 mAdc ± 5%.

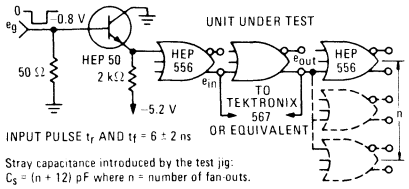
HEP 556 – ECL 3–INPUT GATE

Expandable 3-input gates that provide the positive logic "NOR" function and its complement simultaneously.

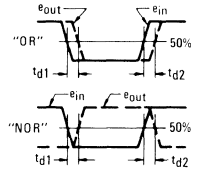
Case 71



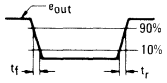
SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY

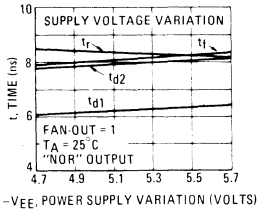


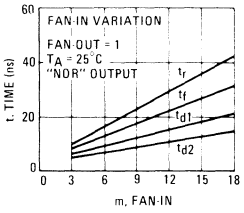
RISE & FALL TIMES



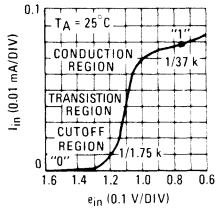
Fan-in obtained with MC355 input expanders; all but driven input connected to −5.2 V.

TYPICAL SWITCHING TIME VARIATIONS

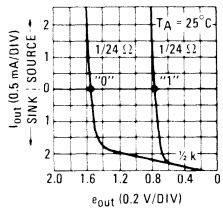




TYPICAL INPUT CHARACTERISTICS

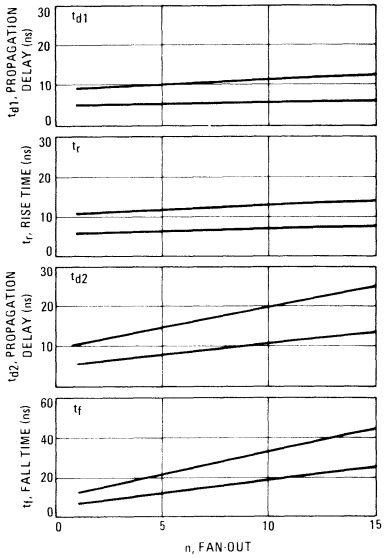


TYPICAL OUTPUT CHARACTERISTICS

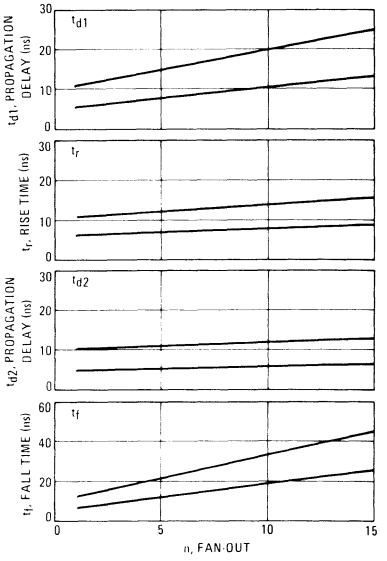


SWITCHING CHARACTERISTICS (10% TO 90% DISTRIBUTION @ 25°C)

"NOR" OUTPUT



"OR" OUTPUT



ELECTRICAL CHARACTERISTICS

@ Test Temperature +25°C	Test Conditions Vdc ± 1%									Test Limits +25°C		
	−0.670	−0.795	−1.350	−5.20	−1.15							
Characteristic	V_H Pin No	V_l max Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Min	Max	Unit
Power Supply Drain Current HEP556	–	–	–	2,6,7,8	1	–	–	3	I_E (2)	–	8.85	mAdc
Power Supply Drain Current HEP557	–	–	–	2,6,7,8	1	–	–	3	I_E (2)	–	3.6	mAdc
Input Current	6	–	–	2,7,8	1	–	–	3	I_{in} (6)	–	100	μAdc
	7	–	–	2,6,8	1	–	–	3	I_{in} (7)	–	↓	↓
	8	–	–	2,6,7	1	–	–	3	I_{in} (8)	–		
"NOR" Logical "1" Output Voltage	–	–	6	2,7,8	1	–	–	3	V_l (5)	−0.670	−0.795	Vdc
	–	–	7	2,6,8	1	–	–	3	V_l (5)	↓	↓	↓
	–	–	8	2,6,7	1	–	–	3	V_l (5)			
"NOR" Logical "0" Output Voltage	–	6	–	2,7,8	1	–	–	3	V_4 (5)	−1.465	−1.750	Vdc
	–	7	–	2,6,8	1	–	–	3	V_4 (5)	↓	↓	↓
	–	8	–	2,6,7	1	–	–	3	V_4 (5)			
"OR" Logical "1" Output Voltage	–	6	–	2,7,8	1	–	–	3	V_5 (4)	−0.670	−0.795	Vdc
	–	7	–	2,6,8	1	–	–	3	V_5 (4)	↓	↓	↓
	–	8	–	2,6,7	1	–	–	3	V_5 (4)			
"OR" Logical "0" Output Voltage	–	–	6	2,7,8	1	–	–	3	V_2 (4)	−1.465	−1.750	Vdc
	–	–	7	2,6,8	1	–	–	3	V_2 (4)	↓	↓	↓
	–	–	8	2,6,7	1	–	–	3	V_2 (4)			
"NOR" Output Voltage Change (No load to full load)	–	–	6	2,7,8	1	–	5 ②	3	$\triangle V_l$ (5)	–	−0.055	Volts
"OR" Output Voltage Change (No load to full load)	–	6	–	2,7,8	1	–	4 ②	3	$\triangle V_5$ (4)	–	−0.055	Volts
"NOR" Saturation Breakpoint Voltage	–	–	–	2,7,8	1	6 ①	–	3	V_3 (5)	–	−0.55	Vdc
	–	–	–	2,6,8	1	7 ①	–	3	V_3 (5)	–	↓	↓
	–	–	–	2,6,7	1	8 ①	–	3	V_3 (5)	–		
Switching Times	Pulse In	Pulse Out								Typ	Max	
Propagation Delay Time	6	4	–	2,7,8	1	–	–	3	t_{d1} (4)	8.5	11.5	ns
	6	5	–	2,7,8	1	–	–	3	t_{d1} (5)	6.5	10.5	↓
	6	4	–	2,7,8	1	–	–	3	t_{d2} (4)	6.0	11.0	
	6	5	–	2,7,8	1	–	–	3	t_{d2} (5)	8.5	11.5	
Rise Time	6	4	–	2,7,8	1	–	–	3	t_r (4)	7.0	11.5	
	6	5	–	2,7,8	1	–	–	3	t_r (5)	9.5	12.5	
Fall Time	6	4	–	2,7,8	1	–	–	3	t_f (4)	9.5	14.0	
	6	5	–	2,7,8	1	–	–	3	t_f (5)	9.0	14.0	↓

Pins not listed are left open

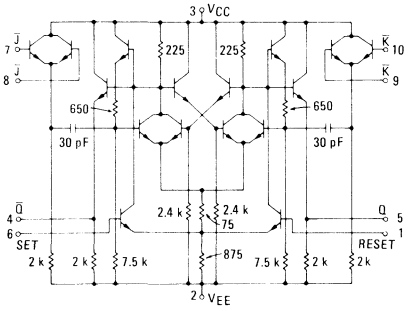
① Input voltage is adjusted to obtain dV "NOR"/dV_{in} = 0.

② Current test conditions: no load = 0; full load = -2.5mAdc ± 5%.

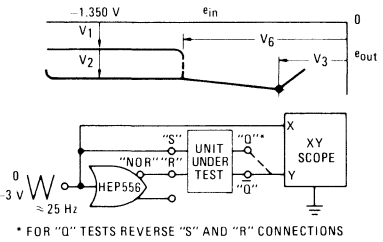
HEP 558 — ECL J-K FLIP-FLOP

AC-coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.

Case 71



TRANSFER CHARACTERISTICS



* FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

FIGURE 1
SWITCHING TIME TEST CIRCUIT

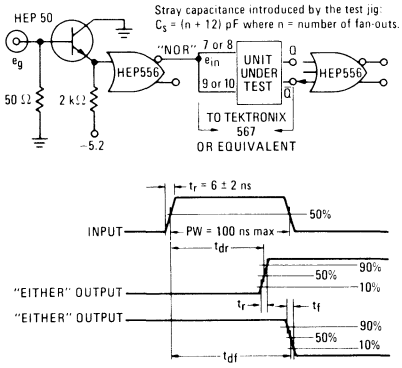
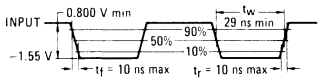


FIGURE 2
INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY



SWITCHING CHARACTERISTICS (10% TO 90% DISTRIBUTION @ 25°C)

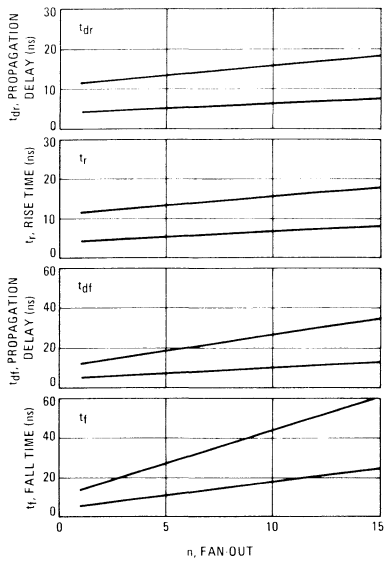


FIGURE 3
SENSITIVITY (NO TOGGLE)

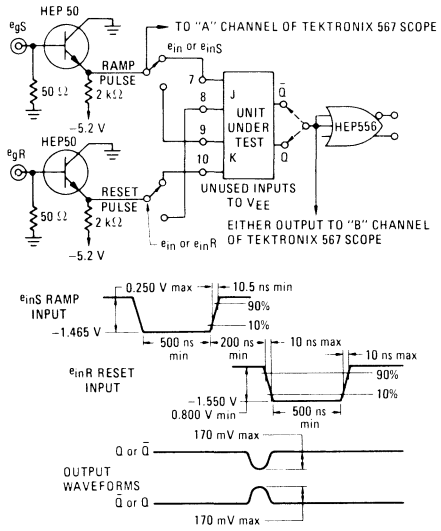
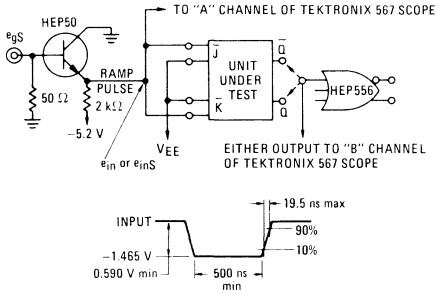


FIGURE 4
SENSITIVITY (TOGGLE)



ELECTRICAL CHARACTERISTICS

@ Test Temperature +25°C	Test Conditions Vdc ± 1%							Symbol	Test Limits +25°C		
	−0.670	−0.795	−1.350	−5.20							
Characteristic	V_H Pin No	V_I max Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Pin No in ( )	Min	Max	Unit
Power Supply Drain Current	–	7,10	–	1,2,6,8,9	–	–	3	I_E (2)	–	21.0	mAdc
Input Current	7	–	–	1,2,6,8,9,10	–	–	3	I_{in} (7)	–	100	μAdc
	8	–	–	1,2,6,7,9,10	–	–	3	I_{in} (8)	–	↓	↓
	9	–	–	1,2,6,7,8,10	–	–	3	I_{in} (9)	–		
	10	–	–	1,2,6,7,8,9	–	–	3	I_{in} (10)	–		
"Q" Logical "1" Output Voltage	–	–	6	1,2,7,8,9,10	–	–	3	V_1 (5)	−0.670	−0.795	Vdc
"Q" Logical "0" Output Voltage	–	–	1	2,6,7,8,9,10	–	–	3	V_2 (5)	−1.465	−1.750	Vdc
"$\bar{Q}$" Logical "1" Output Voltage	–	–	1	2,6,7,8,9,10	–	–	3	V_1 (4)	−0.670	−0.795	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	–	–	6	1,2,7,8,9,10	–	–	3	V_2 (4)	−1.465	−1.750	Vdc
"Q" Output Voltage Change	–	6	–	1,2,7,8,9,10	–	5②	3	$\triangle V_1$ (5)	–	−0.065	Volts
"$\bar{Q}$" Output Voltage Change	–	1	–	2,6,7,8,9,10	–	4②	3	$\triangle V_1$ (4)	–	−0.065	Volts
"Q" Saturation Breakpoint Voltage	–	–	–	1,2,7,8,9,10	6①	–	3	V_3 (5)	–	− 0.65	Vdc
"$\bar{Q}$" Saturation Breakpoint Voltage	–	–	–	2,6,7,8,9,10	1①	–	3	V_3 (4)	–	− 0.65	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	–	–	–	2,7,8,9,10	1.6④	–	3	V_6 (1.6)	− 1.09	− 1.21	Vdc
	Pulse In	Pulse Out									
Toggle Frequency (See Figures 1 and 2)	7,10	5		1,2,6,9	–	–	3	f_{Tog}	15	–	MHz
Sensivity (No Toggle)	7,10	4		1,2,6,8,9	–	–	3	← See Figure 3 →			
	8,9	5		1,2,6,7,10	–	–	3	← See Figure 3 →			
Sensitivity (Toggle)	7,10	4,5		1,2,6,8,9	–	–	3	← See Figure 4 →			
Switching Times									Typ	Max	
Propagation Delay	7,10	4,5		1,2,6,8,9	–	–	3	t_{dr} (4,5)	7.5	13.0	ns
	7,10	4,5		1,2,6,8,9	–	–	3	t_{df} (4,5)	10.0	15.0	↓
Rise Time	7,10	4,5		1,2,6,8,9	–	–	3	t_r (4,5)	8.0	13.0	
Fall Time	7,10	4,5		1,2,6,8,9	–	–	3	t_f (4,5)	11.0	15.5	

Pins not listed are left open

① Input voltage is adjusted to obtain dV_{out}/dV_{in} = "0".

② Current test conditions: no load = 0 to full load = 2.5 mAdc ± 5%.

③ Apply momentary $V_{I\ max}$ to set output, then V_{in} from measurement

④ Input voltage is adjusted to obtain $dV_I/dV_{in} = \infty$

GENERAL RTL AND mW RTL INFORMATION

Resistor-Transistor-Logic (RTL) was the original intergrated logic form, introduced around 1960. The basic circuit is a direct translation of the discrete design into integrated form. RTL is probably the most familiar logic family, is very easy to implement, and offers unusual flexibility. Due to the basic design, it is possible to use RTL devices in linear applications as well as digital.

MAXIMUM RATINGS (T_A @ 25°C)

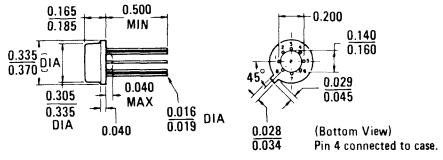
Rating	Symbol	Value	Unit
Input Voltage	–	±4.0	Vdc
Power Supply Voltage (Pulsed ≤1.0s)	–	+12	Vdc
Operating Temperature Range	T_A	+15 to +55	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

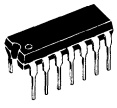
TEST CONDITION TOLERANCES

V_{BOT} = ±10 mV V_{on} = ±2 mV
V_{CC} = ±10 mV V_{off} = ±2 mV
V_{in} = ±2 mV V_{LL} = ±2 mV
V_R = ±1%

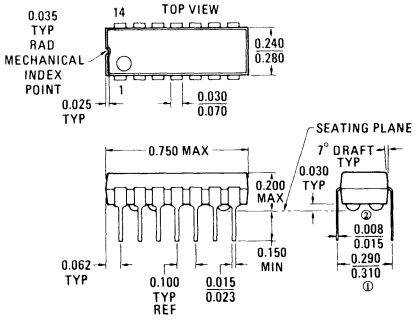
PACKAGING HEP RTL & mW RTL devices are packaged in case type TO-99 (metal) or type TO-116 (epoxy). Specific cases for individual devices are shown below.

TO-99





TO-116



① This dimension is measured at the seating plane.
② 4 insulating stand-offs are provided.

DEFINITIONS

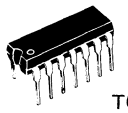
I_{A2},I_{A3}, I_{A4},I_{A5}, I_{A10},I_{A13}, I_{A16}	Minimum available output current from a device with an output loading factor of 2, 3, 4, 5, 10, 13, and 16 respectively. Output voltage not to fall below the value of V_{in}.
I_{AB}	Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.
I_{AM}	The maximum available current from the output of a Dual Gate.
I_{CEX}	Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.
I_{in}	Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.
$1.8I_{in}$	Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.
$2I_{in}$	Maximum input current drawn by one input of a device with 2 bases internally tied together.
I_L	Isolation leakage current.
I_o	Output load current.
V_{BOT}	A high value voltage applied to an input of a device to insure saturation of the driven transistor.
V_{CC}	Supply voltage.
$V_{CE(sat)}$	Maximum saturation voltage with V_{BOT} applied to the input.
V_{in}	Minimum high level voltage applied to the input of a device.
V_{LL}	A supply voltage low enough to allow flow of leakage currents only.
V_{off}	The maximum voltage which may be applied to an input terminal without turning the transistor on.
V_{on}	The minimum voltage which may be applied to an input terminal that will turn the transistor on.
V_{out}	The maximum output voltage with V_{on} applied to the input.
V_R	Value of external resistor connected to V_{CC} for test purposes. V_{RH} = highest node resistor value; V_{RL} = lowest node resistor value

GENERAL RULES

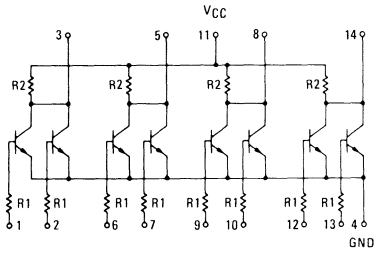
- The number of load circuits that may be driven from an output is determined by the ouput loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- When mixing RTL and mW RTL in the same system, the loading factors must be normalized in accordance with the input current of the units being driven.
- All unused inputs should be returned to ground.

HEP 570 – RTL QUAD 2–INPUT GATE

Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

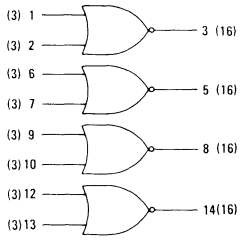


TO-116



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

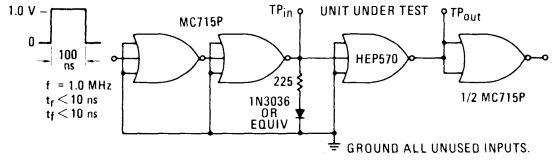
t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

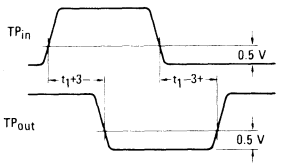


$3 = \overline{1 + 2}$

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
+15°C	0.865	0.865	1.80	0.475	3.60
+25°C	0.850	0.850	1.80	0.460	3.60
+55°C	0.800	0.800	1.80	0.430	3.60

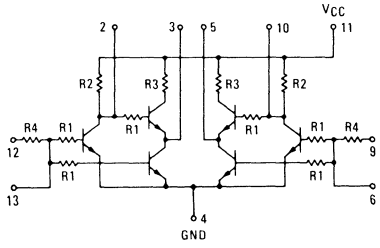
Characteristic	Symbol	Pin Under Test	Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	–	500	–	500	–	470	μAdc	1	–	2	–	11	4
		2	–	500	–	500	–	470	μAdc	2	–	1	–	11	4
Output Current	I_{A5}*	3	2.65	–	2.65	–	2.50	–	mAdc	–	3	–	1,2	11	4
Output Voltage	V_{out}	3	–	400	–	300	–	320	mVdc	–	1	–	–	11	2,4
		3	–	400	–	300	–	320	mVdc	–	2	–	–	11	1,4
Saturation Voltage	$V_{CE(sat)}$	3	–	300	–	290	–	320	mVdc	–	–	1	–	11	2,4
		3	–	300	–	290	–	320	mVdc	–	–	2	–	11	1,4
Switching Time	$t_{on} + t_{off}$	1,3	–	–	–	48	–	–	ns	Pulse In 1	Pulse Out 3	–	–	11	2,4

Ground input pins of gates not under test. Other pins not listed are left open. *I_{A16} is symbol for HEP570.

HEP 571 – RTL DUAL BUFFER

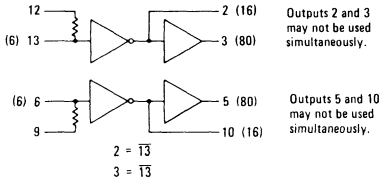
The dual buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input the differentiation of input waveforms and various multivibrator applications.

TO-116



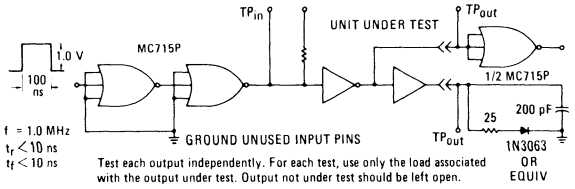
TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 = 100 Ω
R2 = 640 Ω R4 = 1.0 k

t_{pd} = 15 ns
P_D = 50 mW (Input High)
90 mW (Inputs Low)

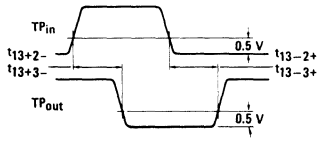


NUMBER IN PARENTHESIS INDICATES LOADING FACTOR.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

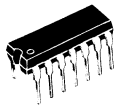
@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
+15°C	0.865	0.865	1.80	0.475	3.60	640
+25°C	0.850	0.850	1.80	0.460	3.60	640
+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	13	-	1.0	-	1.0	-	0.94	mAdc	13	-	-	-	11	-	4
Output Current	I_{A5}	2	2.65	-	2.65	-	2.50	-	mAdc	-	2	-	13	11	-	4
	I_{A8}	3	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	13	11	-	4
Output Voltage	V_{out}	2	-	400	-	300	-	320	mVdc	-	13	-	-	11	-	4
		3	-	400	-	300	-	320	mVdc	-	13	-	-	11	3	4
Saturation Voltage	$V_{CE(sat)}$	2	-	300	-	290	-	320	mVdc	-	-	13	-	11	-	4
		2	-	300	-	290	-	320	mVdc	-	-	-	-	11,12	-	4
		3	-	300	-	290	-	320	mVdc	-	-	13	-	11	3	4
										Pulse In	Pulse Out					
Switching Time	t	13+3–	-	-	-	30	-	-	ns	13	3	-	-	11	-	4
		13–3+	-	-	-	45	-	-	ns	13	3	-	-	11	-	4
		13+2–	-	-	-	28	-	-	ns	13	2	-	-	11	-	4
		13–2+	-	-	-	32	-	-	ns	13	2	-	-	11	-	4

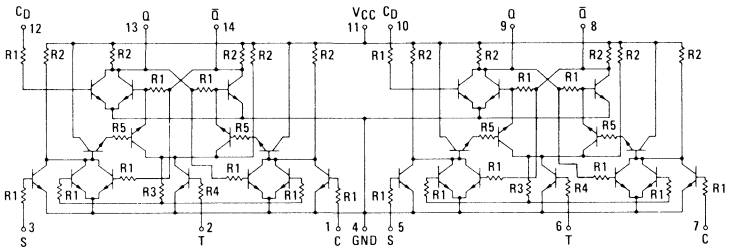
*Ground all unused input pins. Other pins not listed are left open. *Resistor Value to V_{CC}.

HEP 572 – RTL DUAL J-K FLIP-FLOP

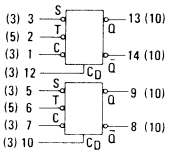
Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



TO-116



TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 = 510 Ω
R2 = 640 Ω R4 = 225 Ω
R5 = 300 Ω



NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

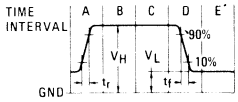
f_{Tog} = 4 MHz
P_D = 182 mW

CLOCKED INPUT OPERATION①

t_n ②		t_{n+1} ②	
S	C	Q	Q̄
1	1	Q_n ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	Q_n	Q_n ③

1. Direct input (CD) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be ≤100 ns.

FIGURE 1
CLOCK PULSE DEFINITION

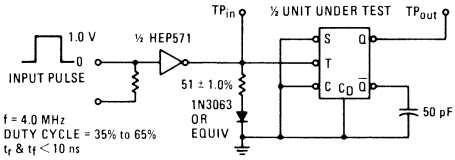


T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+ 0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+ 0.850 V ± 2.0 mV

SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be <1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2
TOGGLE MODE TEST CIRCUIT



FREQUENCY AT TP_{out} SHOULD BE ½ THE FREQUENCY AT TP_{in}

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
+15°C	0.865	0.865	1.80	0.475	3.60
+25°C	0.850	0.850	1.80	0.460	3.60
+55°C	0.800	0.800	1.80	0.430	3.60

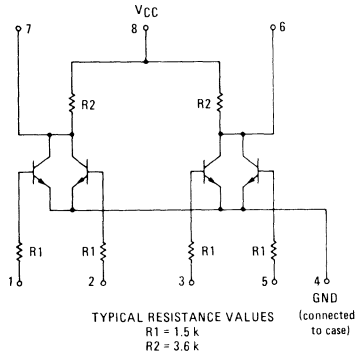
Characteristic	Symbol	Pin Under Test	Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	–	500	–	500	–	470	μAdc	1	–	13	–	11	2,3,4,12
	$2I_{in}$	2	–	1000	–	1000	–	940	↓	2	–	1,3	–	↓	4,12
	I_{in}	3	–	500	–	500	–	470		3	–	14	–		1,2,4,12
	I_{in}	12	–	500	–	500	–	470		12	–	14	–		1,2,3,4
Output Current	I_{A10}	13	1.65	–	1.65	–	1.56	–	mAdc	–	13	1	12	11	2,3,4
		14	↓	–	↓	–	↓	–	↓	–	14	3,12	–	↓	1,2,4
		14		–		–		–		–	12,14	3	–		1,2,4
Output Voltage	V_{out}	13	–	400	–	300	–	320	mVdc	–	12	–	–	11	1,2,3,4,14
		13*#	–	↓	–	↓	–	↓	↓	–	1,3	–	–	↓	4,12
		13*##	–		–		–			–	1	–	3		↓
		13*##	–		–		–			–	–	–	1,3		
		14*##	–		–		–			–	1,3	–	–		
		14*#	–		–		–			–	3	–	1		
		14*#	–	↓	–	↓	–	↓	↓	–	–	–	1,3	↓	↓
Saturation Voltage	$V_{CE(sat)}$	13	–	300	–	290	–	320	mVdc	–	–	12	–	11	1,2,3,4,14
		13#	–	↓	–	↓	–	↓	↓	–	–	–	–	↓	1,2,3,4,12
		14##	–		–		–			–	–	12	–		1,2,3,4

Ground unused input pins. Other pins not listed are left open.
*Clock pulse to pin 2, see Figure 1. #Pin 13 = LOW } Set by a momentary ground prior to the
ξI_{A10} is symbol for MC790P ##Pin 14 = LOW } application of the negative-going Clock Pulse.

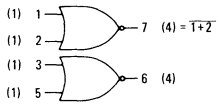
HEP 580 – mW RTL 2–INPUT GATE

Two 2-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

TO-99

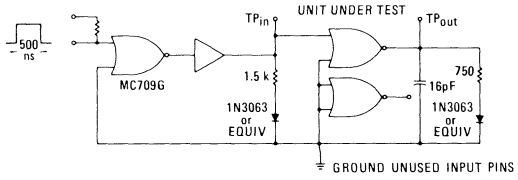


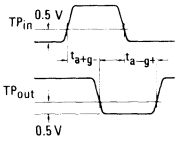
TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k



NUMBERS IN PARENTHESIS INDICATES LOADING FACTOR.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
+25°C	0.830	0.800	1.80	0.460	3.60

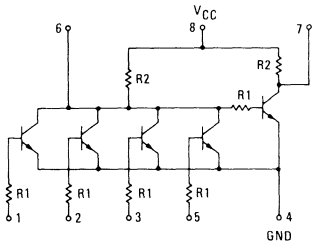
Characteristic	Symbol	Pin Under Test	TEST LIMITS +25°C Min	TEST LIMITS +25°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	–	140	μAdc	1	-	2	-	8	4
		2	–	140	μAdc	2	-	1	-	8	4
Output Current	I_{A4}	7	570	–	μAdc	7	-	3	1,2	8	4
	I_{AM}	7	–	–	–	7	-	3	1,2	8	4
Output Voltage	V_{out}	7	–	350	mVdc	-	1	-	-	8	2,4
		7	–	350	mVdc	-	2	-	-	8	1,4
Saturation Voltage	$V_{CE(sat)}$	7	–	250	mVdc	1	-	-	-	8	2,4
		7	–	250	mVdc	2	-	-	-	8	1,4
Isolation Leakage Current	I_L	8	–	100	μAdc	-	-	-	-	8	1,2,4
Switching Time	t	1 + 7 –	–	50	ns	Pulse In: 1	Pulse Out: 7	-	-	8	4
		1 – 7 +	–	40	ns	1	7	-	-	8	4

Ground input pins of gate not under test. Other pins not listed are left open.

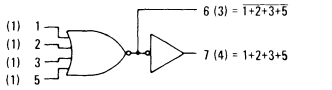
HEP 581 – mW RTL 4–INPUT GATE

Provides the positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).

TO-99

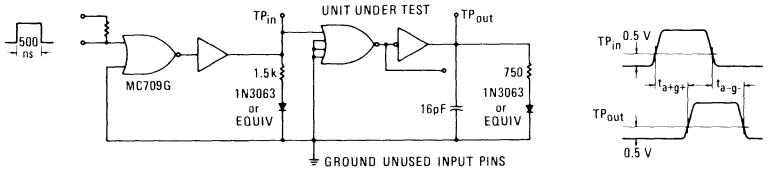


TYPICAL RESISTANCE VALUES
R1 = 1.5k
R2 = 3.6k



NUMBERS IN PARENTHESIS INDICATES LOADING FACTOR

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_u
+25°C	0.830	0.800	1.80	0.460	3.60	0.400

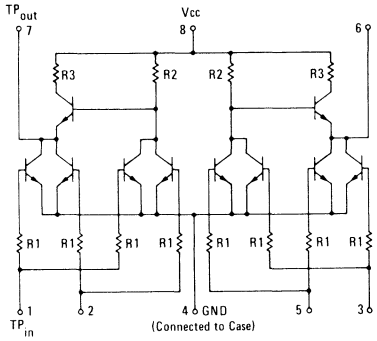
Characteristic	Symbol	Pin Under Test	TEST LIMITS +25°C Min	TEST LIMITS +25°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_u	Gnd
Input Current	I_{in}	1	–	140	μAdc	1	-	2,3,5	-	8	-	4
		2	–	140	μAdc	2	-	2,3,5	-	8	-	4
		3	–	140	μAdc	3	-	1,2,5	-	8	-	4
		5	–	140	μAdc	5	-	1,2,3	-	8	-	4
Output Current	I_{A3}	6	430	–	μAdc	6	-	-	1,2,3,5	8	-	4
	I_{A4}	7	570	–	μAdc	7	-	-	6	8	-	1,2,3,4,5
	I_{AM}	7	–	–	–	7	-	-	6	8	-	1,2,3,4,5
Output Voltage	V_{out}	6	–	350	mVdc	-	1	-	-	8	-	2,3,4,5
		6	–	350	mVdc	-	2	-	-	8	-	1,3,4,5
		6	–	350	mVdc	-	3	-	-	8	-	1,2,4,5
		6	–	350	mVdc	-	5	-	-	8	-	1,2,3,4
		7	–	350	mVdc	-	6	-	-	8	-	1,2,3,4,5
Saturation Voltage	$V_{CE(sat)}$	6	–	250	mVdc	1	-	-	-	8	-	2,3,4,5
		6	–	250	mVdc	2	-	-	-	8	-	1,3,4,5
		6	–	250	mVdc	3	-	-	-	8	-	1,2,4,5
		6	–	250	mVdc	5	-	-	-	8	-	1,2,3,4
		7	–	250	mVdc	6	-	-	-	8	-	1,2,3,4,5
Isolation Leakage Current	I_L	8	–	100	μAdc	-	-	-	-	-	8	1,2,3,4,5
						Pulse In	Pulse Out					
Switching Time	t	1 + 7 +	–	90	ns	1	7	-	-	8	-	2,3,4,5
		1 – 7 –	–	70	ns	1	7	-	-	8	-	2,3,4,5

Pins not listed are left open.

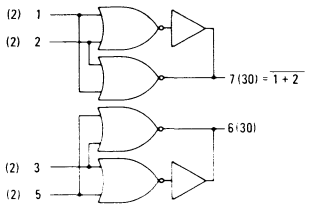
HEP 582 – mW RTL DUAL BUFFER

These buffers are designed to drive a greater number of loads than the basic RTL circuit.

TO-99

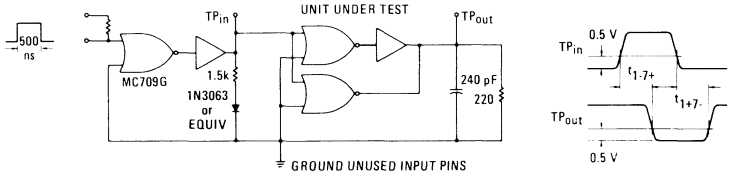


TYPICAL RESISTANCE VALUES
R1 = 1.5k
R2 = 3.6k
R3 = 100



NUMBERS IN PARENTHESIS INDICATES LOADING FACTOR

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

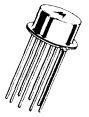
@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(kΩ)
+25°C	0.830	0.800	1.80	0.460	3.60	4.3

Characteristic	Symbol	Pin Under Test	TEST LIMITS +25°C Min	Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{RH}*	Gnd
Input Current	$2I_{in}$	1	–	280	μAdc	1	-	2	-	8	-	4
		2	–	280	μAdc	2	-	1	-	8	-	4
Output Current	I_{AB}	7	4.5	–	mAdc	7	-	-	1,2	8	-	4
Ouput Voltage	V_{out}	7	–	350	mVdc	-	1	-	-	8	7	2,4
		7	–	350	mVdc	-	2	-	-	8	7	1,4
Saturation Voltage	$V_{CE(sat)}$	7	–	250	mVdc	1	-	-	-	8	7	2,4
		7	–	250	mVdc	2	-	-	-	8	7	1,4
Isolation Leakage Current	I_L	8	–	100	μAdc	-	-	-	-	8	-	1,2,3,4,5
Switching Time	t	1 + 7 –	–	90	ns	Pulse In 1	Pulse Out 7	-	-	8	-	2,4
		1 – 7 +	–	70	ns	1	7	-	-	8	-	2,4

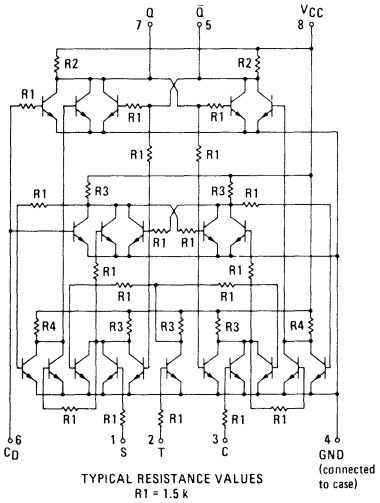
Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

HEP 583 — mW RTL J-K FLIP-FLOP

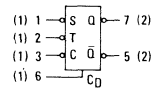
J-K Flip-Flop with a direct clear input in addition to the clocked inputs.



TO-99



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k
R3 = 4.5 k
R4 = 7.2 k



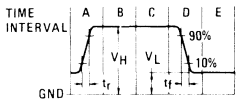
NUMBERS IN PARENTHESIS INDICATE LOADING FACTOR

CLOCKED INPUT OPERATION ①

t_n ②		t_{n+1} ②	
S	C	Q	Q̄
1	1	Q_n ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ③

1. Direct input (CD) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be <100 ns.

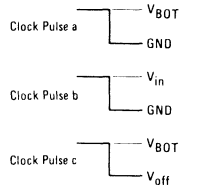
FIGURE 1a CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

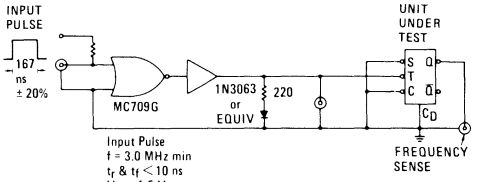
A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be <1.0 µs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 1b CORRELATION OF CLOCK PULSE a, b & c



The negative transition of Clock Pulse a must precede the negative transition of Clock Pulse b.

FIGURE 2 TOGGLE MODE TEST CIRCUIT

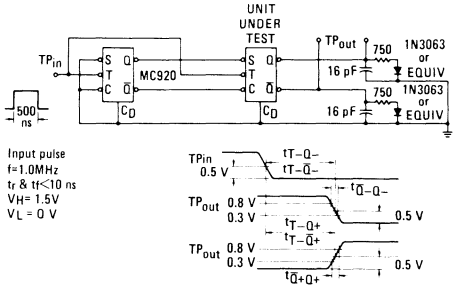


Input Pulse
f = 3.0 MHz min
t_r & t_f < 10 ns
V_H = 1.5 V
V_L = 0 V

Sense frequency should be ½ that of Input Pulse

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

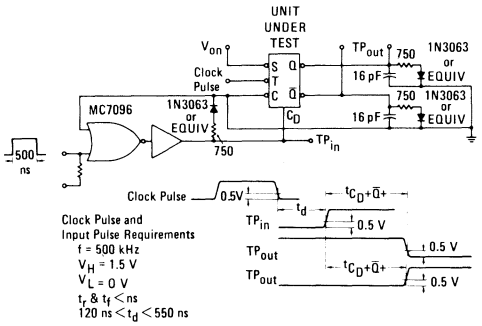
FIGURE 3a



SWITCHING TIMES

Test	Fig. No.	ns@ +25°C min	ns@ +25°C max
t_{T-Q-}	3A	40	140
t_{T-Q+}	3A	70	195
$t_{T-\bar{Q}-}$	3A	40	140
$t_{T-\bar{Q}+}$	3A	70	195
$t_{\bar{Q}+Q+}$	3A	30	100
$t_{\bar{Q}-Q-}$	3A	5	40
t_{CD+Q-}	3B	55	----
$t_{CD+\bar{Q}+}$	3B	5	----

FIGURE 3b



Clock Pulse and Input Pulse Requirements
f = 500 kHz
V_H = 1.5 V
V_L = 0 V
t_r & t_f < ns
120 ns < t_d < 550 ns

ELECTRICAL CHARACTERISTICS

@Test Temperature +25°C

TEST VOLTAGE VALUES (Volts)				
V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
0.830	0.800	1.80	0.460	3.60

Characteristic	Symbol	Pin Under Test	TEST LIMITS +25°C Min	TEST LIMITS +25°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1#*	—	140	µAdc	-	-	3	-	8	4,6
		2	—	140	µAdc	2	-	3	-	8	1,3,4,6
		3*ξ	—	140	µAdc	-	-	1	-	8	4,6
	$2I_{in}$	6	—	280	µAdc	6	-	2,3,5	-	8	4
Output Current	I_{A2}	5*†	290	—	µAdc	-	-	3	-	8	1,4,6
		7*†	290	—	µAdc	-	-	1	-	8	3,4,6
Saturation Voltage	$V_{CE(sat)}$	5*Δ	—	250	mVdc	-	1	-	3	8	4,6
		5**Δ	—	250	MVdc	-	-	-	1,3	8	4,6
		7	—	250	mVdc	-	6	1,2	-	8	3,4,5
		7**◇	—	250	mVdc	-	1,3	-	-	8	4
		7**◇◇	—	250	mVdc	-	3	-	-	8	4,6
		7**◇◇	—	250	mVdc	-	-	-	1,3	8	4,6

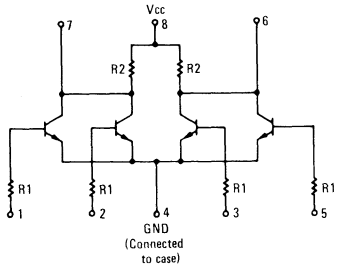
Pins not listed are left open.

* = Pin 2 Clock Pulse a
** = Pin 2 Clock Pulse c
= = Pin 1 Clock Pulse b
ξ = Pin 3 Clock Pulse b
† = Pin 5 Clock Pulse b
‡ = Pin 7 Clock Pulse b (See Figure 1b)
Δ Pin 5 = } Momentary ground prior to negative
ΔΔ Pin 7 = } transition of Clock Pulse c.
◇ Pin 6 = Momentary V_{BOT} prior to negative transition of Clock Pulse c.

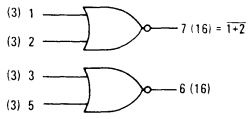
HEP 584 – RTL DUAL 2–INPUT GATE

Two 2-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

TO-99

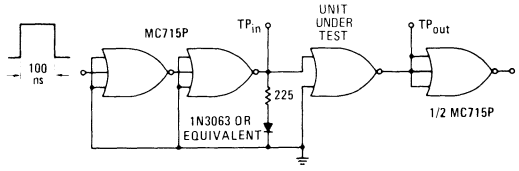


TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

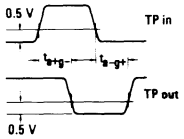


NUMBERS IN PARENTHESIS INDICATES LOADING FACTOR.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



GROUND UNUSED INPUT PINS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

@Test Temperature +25°C	TEST VOLTAGE VALUES (Volts)				
	V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
	0.844	0.844	1.50	0.554	3.00

Characteristic	Symbol	Pin Under Test	TEST LIMITS +25°C Min	TEST LIMITS +25°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	–	450	μAdc	1	-	2	-	8	4
		2	–	450	μAdc	2	-	1	-	8	4
Output Current	I_{A5}	7	2.38	–	mAdc	-	7	-	1,2	8	4
Output Leakage Current	I_{CEX}	7	–	225	μAdc	7	-	-	1,2	8	4
Output Voltage	V_{out}	7	–	400	mVdc	-	1	-	-	8	4
		7	–	400	mVdc	-	2		-	8	4
Saturation Voltage	$V_{CE(sat)}$	7	–	260	mVdc	-	-	1	-	8	4
		7	–	260	mVdc			2		8	4
						Pulse In	Pulse Out				
Switching Time	t	1 + 7 –	–	20	ns	1	7	-	-	8	4
		1 – 7 +	–	28	ns	1	7	-	-	8	4

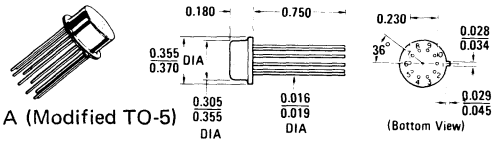
Ground inputs of gate not under test. Pins not listed are left open.

GENERAL LINEAR IC INFORMATION

The HEP linear integrated circuits offers the technician a wide variety of analog devices that are excellent for experimental and prototype work. For example, the HEP590 lends itself very well to either IF or RF AM and FM applications, the HEP591 is good in FM IF and discriminator applications, the HEP592 is a complete stereo preamplifier (external controls and compensation are required), and the HEP593 provides one watt of audio power. Thus, with one HEP592 and two HEP593's, a complete stereo system is quite practical in less space than a pack of cigarettes.

PACKAGING—HEP Linear IC's are packaged in the Motorola case type 71 metal package.

10 LEAD METAL PACKAGE



Case 71—71A (Modified TO-5)

NOTE:
Case 71 has pin 1 under tab, case 71A has pin 10 under tab.

DEFINITIONS

AM_R	AM Rejection (dB)
A_p	Power Gain (dB)
A_v	Voltage Gain (V/V or dB as stated)
A_{VOL}	Open Loop Voltage Gain (V/V or dB as stated)
BW	Bandwidth (Hertz)
$e_{out\ 1}$ $e_{out\ 2}$	Channel Separation (dB)
I_b	Input Bias Current (μA)
I_{CC}	Power Supply Current for V_{CC} (mA)
I_{EE}	Power Supply Current for V_{EE} (mA)
I_{out}	Peak Load Current (Amp)
NF	Noise Figure (dB)
P_D	Power Dissipation (Watts)
P_{out}	Output Power (Watts)
R_{od}	Discriminator Output Resistance (Ohms)
T_A	Ambient Temperature (°C)
T_C	Case Temperature (°C)
THD	Total Harmonic Distortion (%)
t_s	Output Short Circuit Duration (Time)
T_{stg}	Storage Temperature (°C)
V_+	Positive Power Supply Voltage (Volts)
V_-	Negative Power Supply Voltage (Volts)
V_{AGC}	Automatic Gain Control Voltage (Volts)
V_{CC}	Positive Power Supply Voltage (Volts)
V_{EE}	Negative Power Supply Voltage (Volts)
$V_{i(lim)}$	Input Limiting Voltage (μV)
V_{in}	Differential Input Signal (Volts)
V_{oaf}	Recovered Audio Output Voltage (mV)
V_{out}	Output Voltage Swing (Vp-p)
Z_{in}	Input Impedance (Ohms)
Z_{out}	Output Impedance (Ohms)

POWER SUPPLIES FOR THE HEP 592 & HEP 593

Since the HEP 592 and 593 ICs shown on pages 24 and 26 require both a positive and a negative supply voltage, the following circuits and information is included. It should be noted that the split supply in Figure 1 is the most desirable from the standpoint of long and efficient operation.

SPLIT SUPPLY

The requirements for the power supply are not too critical. A suitable supply using a center-taped transformer is shown in Figure 1. Each integrated circuit requires about 15 mA of current. The simple shunt zener regulator uses the HEP103, which has a dynamic impedance of about 3 Ω at 41 mA. Any ripple that may be present on the filter capacitor will be reduced by a factor of about 15 which corresponds to about 35 dB. The HEP592 or 593 is relatively insensitive to hum and the few hundred microvolts present with this supply is not objectionable. Resistors RB and RC are used to limit surge current due to the initial charging of CA and CB.

The resistor RS is computed using:

$$RS = \frac{V_Z}{\text{total } I_{av} + I_Z}$$

where I_{av} = 15 mA for each HEP592 and 400 mA for each HEP593 operating class A.

The zener tolerance is ± 10%, which is sufficient since the IC is also tolerant of supply voltage variations.

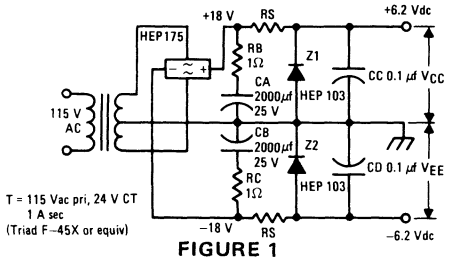


FIGURE 1

SINGLE SUPPLY

Operation from a single rather than a split power supply may be desired. In this event, either of the two methods shown in Figure 2 may be used. Note that IC common is connected, in (a), to the junction of the two zeners, and, in (b), to the junction of the divider resistors RA and RB. This allows each output dc voltage to be at 1/2 V_Z which gives the effect of having a split supply.

The method shown in Figure 2(a) is self explanatory. Use of 10% or 5% tolerance zeners is recommended to prevent variations in the equivalent positive and negative supplies.

The resistor RS is computed using:

$$RS = \frac{tdc - V_Z}{\text{total } I_{av} + I_Z}$$

where I_Z is the current through the zeners. (HEP103 = 41 mA, HEP105 = 21 mA).

The zener current, I_Z,should be chosen to ensure operation of the zeners in their lowest dynamic impedance region.

The method shown in (b) is similar to that shown in (a). The divider resistors are required to supply input bias current to the IC. The maximum input current is 10 μA per IC, so the current through the divider should be at least ten times the total input bias current drawn by all the ICs in the amplifier. The bypass capacitors should then be selected to have a reactance that is at least one-tenth of the resistance of the divider resistors at the lowest frequency of operation of the preamplifier. RS is then computed as before.

In Figure (b), the zener and RS could be eliminated with small loss in performance. The final choice is left up to the designer.

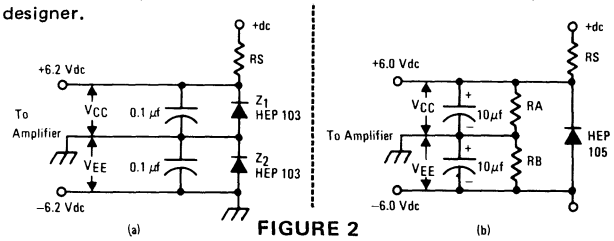


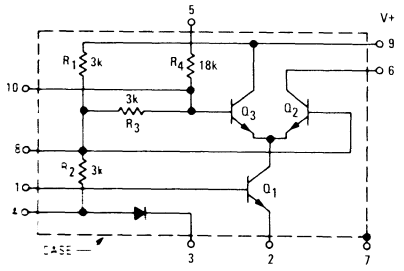
FIGURE 2

HEP 590 — HIGH FREQUENCY RF–IF AMPLIFIER

Typical Amplifier Features:

- Constant Input Impedance over entire AGC range
- Extremely Low y_{12} — 0.001 mmho
- High Power Gain — 30 dB @ 60 MHz (0.5 MHz BW)
- Good Noise Figure — 5.0 dB @ 60 MHz
- High Voltage-Gain — Bandwidth Product — 2.0 GHz

Case 71



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V+	20	Vdc
AGC Supply Voltage	V_{AGC}	20	Vdc
Differential Input Voltage, Pin 1 to Pin 4 (R_S = 500 ohms)	V_{in}	±5	V (RMS)
Power Dissipation (Package Limitation) Derate above 25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	−55 to + 125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

The HEP590 is built with monolithic fabrication techniques utilizing diffused resistors and small-geometry transistors. Excellent AGC performance is obtained by shunting the signal through the AGC transistor Q_3 maintaining the operating point of the input transistor, Q_1. This keeps the input impedance constant over the entire AGC range.

The amplifier is intended to be used in a common-emitter, common-base configuration (Q_1 and Q_2) with Q_3 acting as an AGC transistor. The input signal is applied between pins 1 and 4, where pin 4 is ac-coupled to ground. DC source resistance between pins 1 and 4 should be small (less than 100 ohms). Pins 2 and 3 should be connected together and grounded. Pins 8 and 10 should be bypassed to ground. The positive supply voltage is applied at pin 9 and at higher frequencies, pin 9 should also be bypassed to ground. The output is taken between pins 6 and 9. The substrate is connected to pin 7 and should be grounded. AGC voltage is applied to pin 5.

ELECTRICAL CHARACTERISTICS

Characteristic	Conditions	Figure	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS							
Output Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V_{out}	3.80 5.90	– –	4.65 6.00	Vdc
Test Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V_8	2.85 3.25	– –	3.40 3.80	Vdc
Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_D	– –	– –	2.2 2.5	mAdc
AGC Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_{AGC}	– –	– –	-0.2 0.18	mAdc
SMALL SIGNAL CHARACTERISTICS							
Small-Signal Voltage Gain	f = 500 kHz	2	A_V	22	–	29	dB
Bandwidth		2	BW	22	–	–	MHz
Transducer Power Gain	f = 60 MHz, BW = 6 MHz f = 100 MHz, BW = 6 MHz	3	A_P	– –	25 21	–	dB

FIGURE 1
DC CHARACTERISTICS TEST CIRCUIT

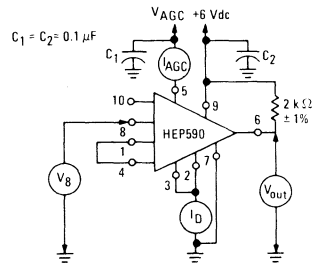
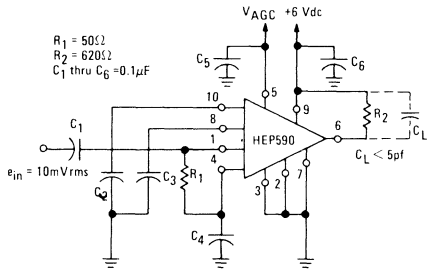


FIGURE 2
VOLTAGE GAIN & BANDWIDTH TEST CIRCUIT



HEP 590 – HIGH FREQUENCY RF–IF AMPLIFIER (Continued)

FIGURE 3
POWER GAIN TEST CIRCUIT @ 60 MHz

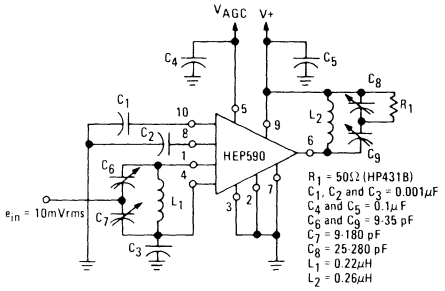


FIGURE 4
DRAIN CURRENT TEMPERATURE CHARACTERISTICS

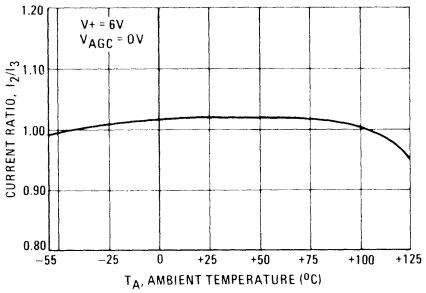


FIGURE 5
INPUT RESISTANCE & CAPACITANCE vs. FREQUENCY

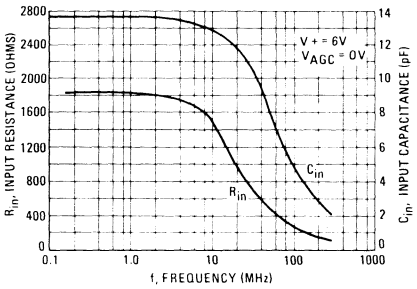


FIGURE 6
INPUT RESISTANCE & CAPACITANCE vs. AGC VOLTAGE

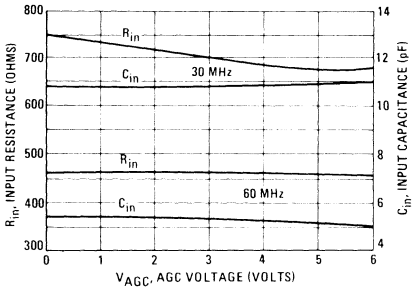


FIGURE 7
OUTPUT RESISTANCE & CAPACITANCE vs. FREQUENCY

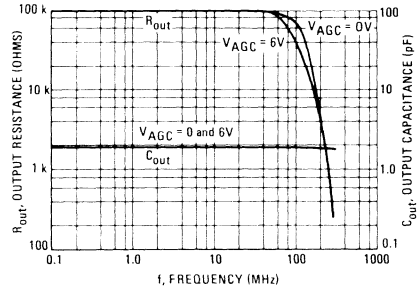


FIGURE 8
OUTPUT RESISTANCE & CAPACITANCE vs. AGC VOLTAGE

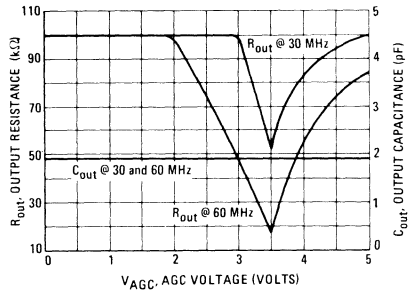


FIGURE 9
FORWARD TRANSFER ADMITTANCE vs. FREQUENCY

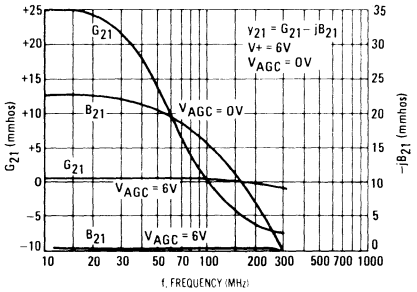


FIGURE 10
FORWARD TRANSFER ADMITTANCE vs. AGC VOLTAGE

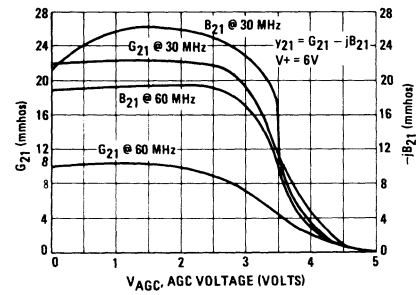


FIGURE 11
MAXIMUM TRANSDUCER
POWER GAIN vs. FREQUENCY

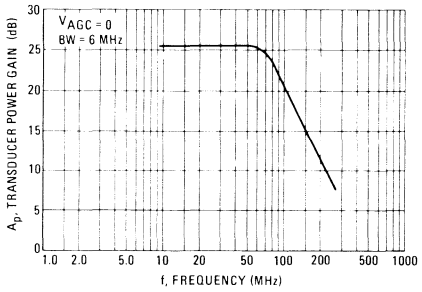


FIGURE 12
TRANSDUCER
POWER GAIN vs. TEMPERATURE

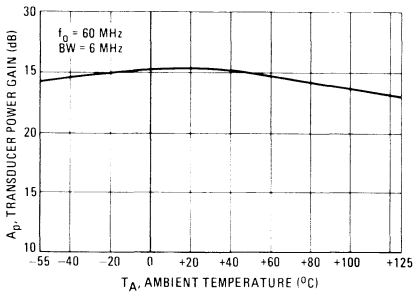


FIGURE 13
TRANSDUCER POWER BANDWIDTH vs. AGC VOLTAGE

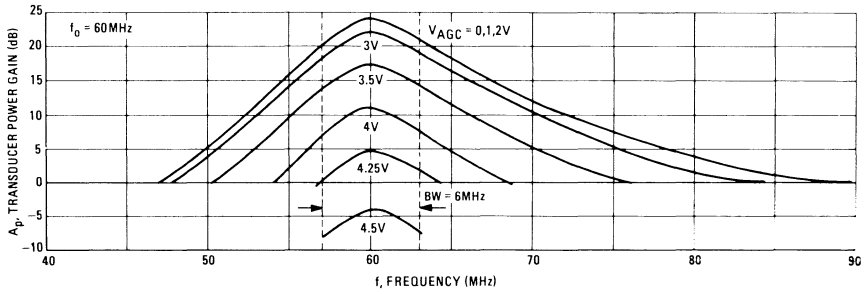


FIGURE 14
NOISE FIGURE & OPTIMUM
SOURCE RESISTANCE vs. FREQUENCY

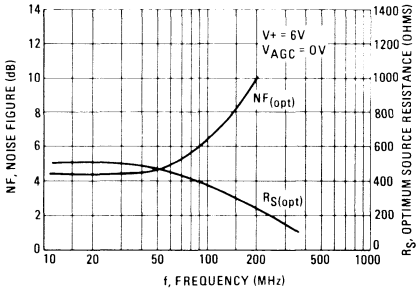
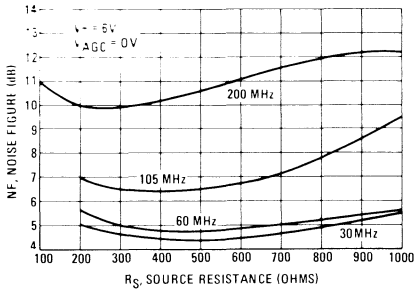


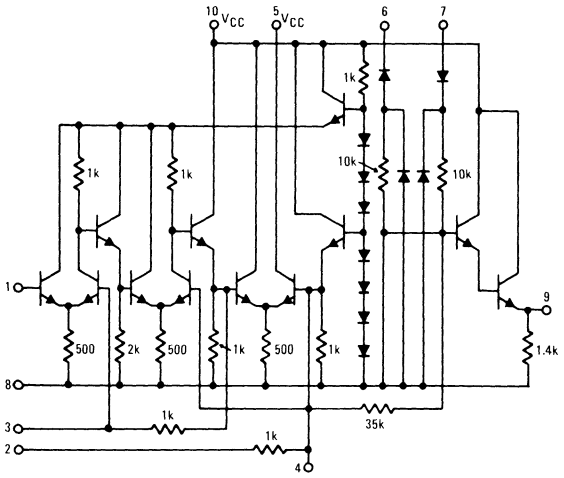
FIGURE 15
NOISE FIGURE vs. SOURCE RESISTANCE



HEP 591 – WIDE BAND AMPLIFIER/DISCRIMINATOR

Ideal for FM IF and discriminator in radio and TV applications, very popular for the ham radio operator and experimenters.

Case 71A



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply Voltage to Pins 10 and 5	V_{CC}	+10	Vdc
Power Dissipation	P_D	600	mW
Derate above 25°C		4.6	mW/°C
Input Signal Voltage	V_{in}	±3	Volts
Operating Temperature	T_A	-55 to + 125	°C
Storage Temperature	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Drain	I_{CC}	12	–	27	mA
Voltage Gain	A_V	60	-	-	dB
Recovered Audio	V_{oaf}				mV
f deviation = 25 kHz		135	–	–	
f deviation = 7.5 kHz		45	–	–	
Total Harmonic Distortion	THD	–	–	2	%
Input Limiting Voltage	$V_{i(lim)}$	–	300	800	μV
Amplitude-Modulation Rejection	AM_R	–	50	–	dB
Discriminator Output Resistance	R_{od}	–	60	–	ohms

FIGURE 1
DC POWER SUPPLY CURRENT DRAIN

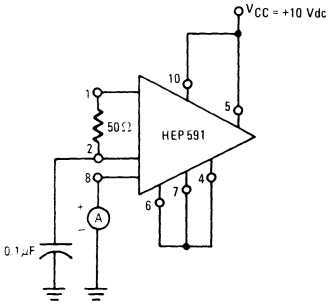


FIGURE 2
VOLTAGE GAIN

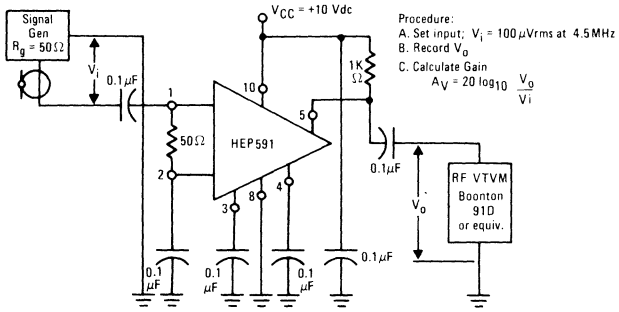
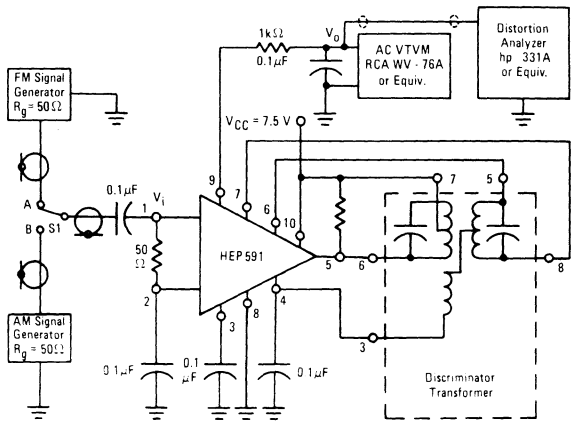


FIGURE 3
TEST CIRCUIT FOR V_o(af), THD, V_i(lim) & AMR



TEST PROCEDURES

A. Recovered Audio Frequency Voltage: Set V_{CC} = 7.5 Vdc. Place switch S_1 in position A. Set input f_i = 4.5 MHz; V_i = 100 mVrms; modulating f_m = 400 Hz; and deviation f_d = ±7.5 kHz. Record V_o(af).

B. Total Harmonic Distortion: Set same as paragraph A except f_d = ± 25 kHz. Record percent THD.

C. Input Limiting Voltage (knee): Set same as paragraph A. Record V_o. Decrease V_i until V_o decreases 3 db. Record V_i(lim).

D. AM Rejection: Set V_{CC} = 7.5 Vdc. Place S_1 in position A. Set input V_i = 10 mV and f_i = 4.5 MHz; modulating f_m = 400 Hz and deviation f_d = ±25 kHz. Record V_o (FM). Place switch S_1 in position B. Set f_i = 4.5 MHz; V_i = 10 mV; f_m = 400 Hz; and modulation = 50%. Record V_o (AM). Calculate AM Rejection = $20 \log 10 \frac{V_o \text{ (FM)}}{V_o \text{ (AM)}}$. Record AMR.

HEP 592 — STEREO PREAMPLIFIER

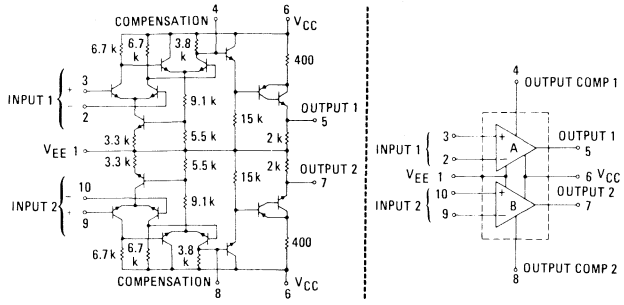
Each Preamplifier Features:

- Low Input Noise Voltage -0.5μV typical
- Large Output Voltage Swing — 4.5 V rms min
- High Open-Loop Voltage Gain = 8,000 min
- Channel Separation = 60 dB min at 10 kHz
- Short-Circuit-Proof Design

Case 71

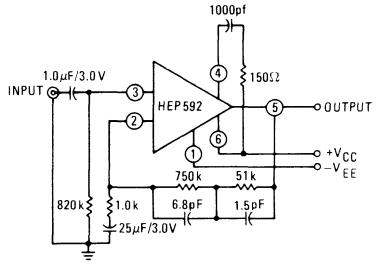
MAXIMUM RATINGS (T_A = 25°C)

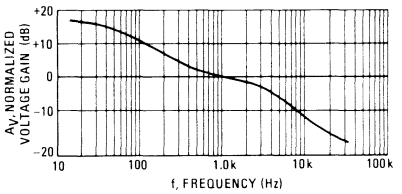
Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8 -8	Vdc Vdc
Input Signal	V_{in}	±2	Volts
Output Short-Circuit Duration	I_S	Continuous	–
Power Dissipation Derate above T_A = 25°C	P_D	400 3.3	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C



TYPICAL PREAMPLIFIER APPLICATIONS

FIGURE 1
MAGNETIC PHONO PLAYBACK PREAMPLIFIER/R IAA EQUALIZED

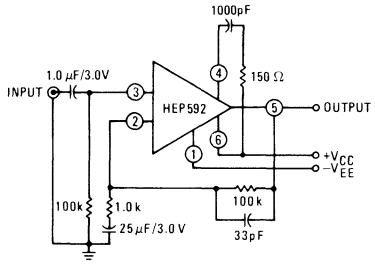


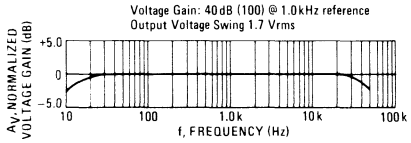


TYPICAL PERFORMANCE CHARACTERISTICS

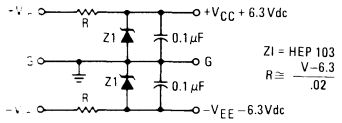
Voltage Gain	34 dB (50) @ 1.0 k Hz
Input Overload Point	30mVrms @ 1.0 k Hz
Output Voltage Swing	1.5 Vrms @ 1.0 k Hz @ 0.1% THD
Output Noise Level	Better Than 70dB Below 10 mV Phono Input (Input Shorted)

FIGURE 2
BROADBAND AUDIO AMPLIFIER





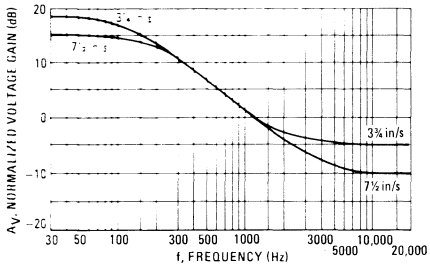
SUGGESTED POWER SUPPLY CIRCUIT

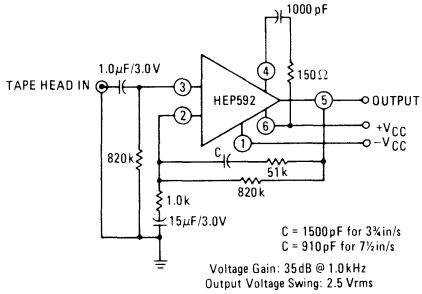


ZI = HEP 103

$R \geq \frac{V-6.3}{.02}$

FIGURE 3
NAB TAPE HEAD EQUALIZATION





C = 1500pF for 3¾in/s
C = 910pF for 7½in/s

Voltage Gain: 35dB @ 1.0kHz
Output Voltage Swing: 2.5 Vrms

FIGURE 4
POWER DISSIPATION vs. SUPPLY VOLTAGE

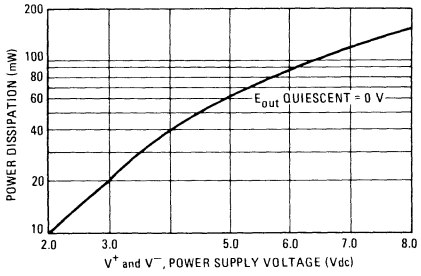


FIGURE 5
OUTPUT LINEARITY

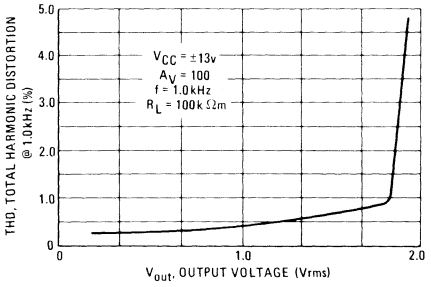
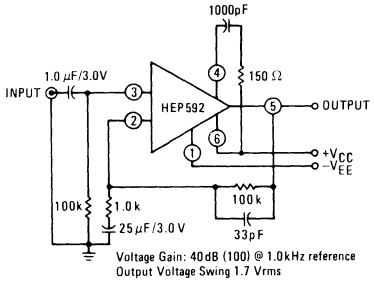
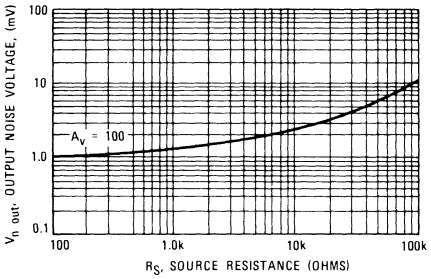


FIGURE 6
OUTPUT NOISE VOLTAGE vs. SOURCE RESISTANCE





ELECTRICAL CHARACTERISTICS

Each Preamplifier
(V^+ = +8 Vdc, V^- = _8 Vdc, T_A = 25°C unless otherwise noted)

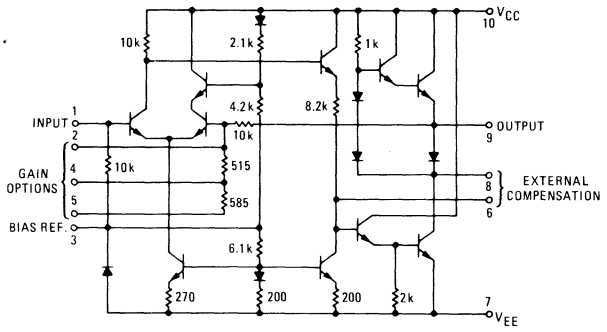
Characteristic Definitions (linear operations)	Characteristic	Symbol	Min	Typ	Max	Unit
$A_{VOL} = \frac{e_{out}}{e_{in}}$	Open Loop Voltage Gain	A_{VOL}	8,000	10,000	12,000	V/V
	Output Voltage Swing (R_L = 10 kΩ)	V_{out}	4.5	5.5	–	V rms
I_2, I_1	Input Bias Current $I_b = \frac{I_1 + I_2}{2}$	I_D	–	1.0	10	μA
I_2, I_1	Input Offset Current ($I_{io} = I_1 - I_2$)	I_{io}	–	0.2	0.4	μA
V_{IO}, V_{out} = 0	Input Offset Voltage	V_{io}	–	1.5	10	mV
	DC Power Dissipation (Power Supply = ± 13 V, V_{out} = 0)	P_D	–	–	400	mW
$e_{out\ 1}$, $e_{out\ 2}$	Channel Separation (f = 10 kHz)	$\frac{e_{out\ 1}}{e_{out\ 2}}$	–	-60	–	db

HEP 593 – AUDIO POWER AMPLIFIER

Typical Amplifier Features:

- Low Total Harmonic Distortion – 0.4% typical at 1.0 Watt
- Low Output Impedance – 0.2 ohm
- Excellent Gain – Temperature Stability

Case 71



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Total Power Supply Voltage	|V+| + |V-|	18	Vdc
Peak Load Current	Iout	0.5	Amp
Audio Output Power	P_{out}	1.8	Watt
Power Dissipation $T_A = 25^\circ C$ Derate above $25^\circ C$ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	 600 4.8 1.8 14.4	 mW mW/°C Watt mW/°C
Operating Temperature Range	T_C	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 μF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 1 and 2, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from The V+ supply to pin 10 can cause high frequency instability. To prevent this, the V+ by-pass capacitor should be connected with short leads from the V+ pin to ground. If this capacitor is remotely located a series R-C network (0.1 μF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 1 and 2.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In application which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CONNECTIONS

FIGURE 1 SPLIT SUPPLY OPERATION

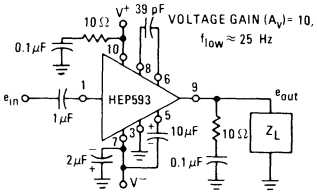
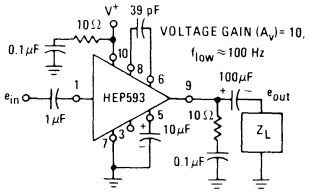
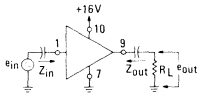
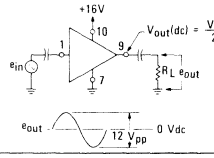
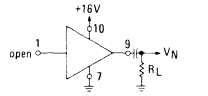
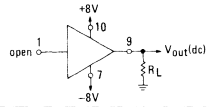
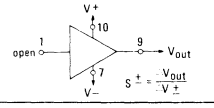


FIGURE 2 SINGLE SUPPLY OPERATION



ELECTRICAL CHARACTERISTICS

Characteristic Definitions	Characteristic	R_L (ohms)	Gain Option*	Symbol	Min	Typ	Max	Unit
	Output Power	16	–	P_{out}	1.0	1.1	–	Watt
	Power Dissipation (@ P_{out} = 1.0 W)	16	–	P_D	–	0.9	1.2	Watt
	Voltage Gain	16 16 16	10 18 36	A_v	8.0 – –	10 18 36	12 – –	V/V
	Input Impedance	–	10	Z_{in}	7.0	10	–	kΩ
	Output Impedance	–	10	Z_{out}	–	0.2	–	Ω
	Power Bandwidth (for e_{out} < 5% THD)	16 16 16	10 18 36		– – –	270 250 210	– – –	kHz
	Total Harmonic Distortion (for e_{in} < 0.05% THD, f = 20 Hz to 20 kHz) P_{out} = 1.0 Watt (sinewave) P_{out} = 0.1 Watt (sinewave)	 16 16	 10 10	THD	 – –	 0.4 0.5	 – –	%
	Zero Signal Current Drain	∞	–	I_D	–	11	15	mAdc
	Output Noise Voltage	16	10	V_n	–	0.3	–	mV RMS
	Output Quiescent Voltage (Split Supply Operation)	16	–	$V_{out(dc)}$	–	±10	±30	mVdc
	Positive Supply Sensitivity (V^- constant)	∞	–	S+	–	-40	–	mV/V
	Negative Supply Sensitivity (V^+ constant)	∞	–	S-	–	-40	–	mV/V

*To obtain the voltage gain characteristics desired, use the following pin connections: A_V = 10; pins 2 & 4 open, pin 5 to ac gnd. A_V = 18; pins 2 & 5 open, pin 4 to ac gnd. A_V = 36; pin 2 connected to pin 5, pin 4 to ac gnd.

FIGURE 3
MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)

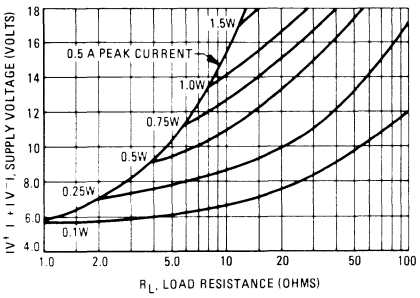


FIGURE 4
MAXIMUM DEVICE DISSIPATION (SINE WAVE)

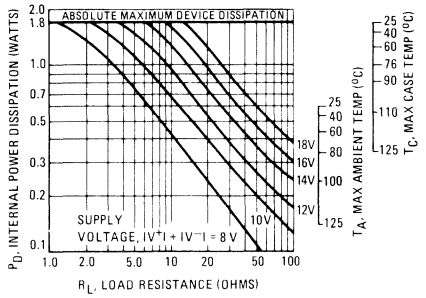


FIGURE 5
TOTAL HARMONIC DISTORTION vs. LOAD RESISTANCE

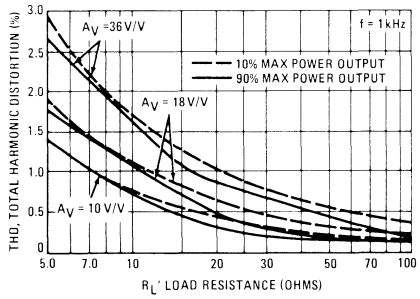


FIGURE 6
TOTAL HARMONIC DISTORTION vs. FREQUENCY

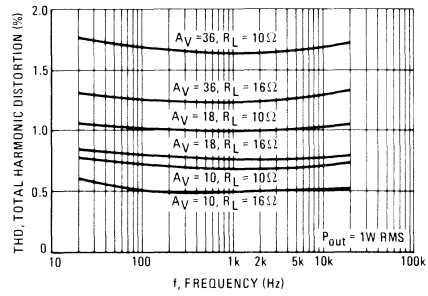


FIGURE 7
VOLTAGE GAIN vs. TEMPERATURE

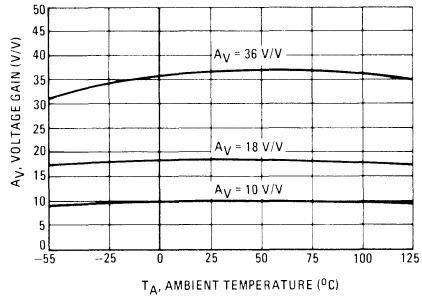


FIGURE 8
OUTPUT VOLTAGE CHANGE

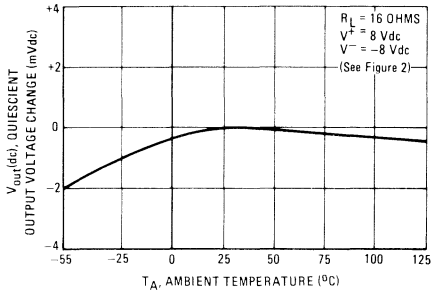


FIGURE 9
VOLTAGE GAIN vs. FREQUENCY (R_L = 16 OHMS)

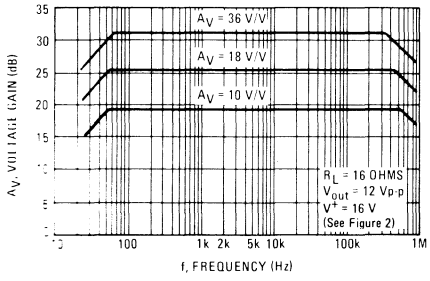
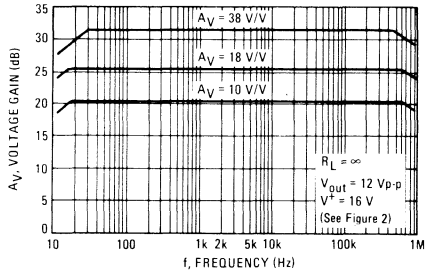


FIGURE 10
VOLTAGE GAIN vs. FREQUENCY (R_L = ∞)



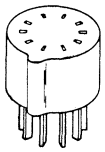
IC CROSS REFERENCE GUIDE

Type to be Replaced	See Note	HEP Replacement	Type to be Replaced	See Note	HEP Replacement	Type to be Replaced	See Note	HEP Replacement
CA3002		590	MC811G		581	SN17811L	1	581
CA3003		590	MC811F	2	581	SW303F	2	553
CA3004		590	MC814G		584	SW303T		553
CA3013		591	MC814F	2	584	SW304F	2	554
CA3014		591	MC817P	1	570	SW304T		554
MC303G		553	MC824P	1	570	SN17810L	2	556
MC303F	2	553	MC876P	1	572	SW306T		556
MC304G		554	MC881G	1	582	SW308F	2	558
MC304F	2	554	MC882G	1	583	SW308T		558
MC306G		556	MC890P	1	572	SW353F	2	553
MC306F	2	556	MC899P	1	571	SW353T		553
MC308G		558	MC910G	1	580	SW354F	2	554
MC308F	2	558	MC910F	1,2	580	SW354T		554
MC353G		553	MC911G	1	581	SW356F	2	556
MC353F	2	553	MC911F	1,2	581	SW356T		556
MC354G		554	MC914G	1	584	SW358F	2	558
MC354F	2	554	MC914F	2	584	SW358T		558
MC356G		556	MC981G	1	582	U3F991129X	2	581
MC356F	2	556	MC982G	1	583	U3F991421X	2	584
MC358G		558	MC1302G		592	U3F991422X	2	584
MC358F	2	558	MC1302P	2	592	U5B991021X		580
MC710G		580	MC1303P	2,3	592	U5B991029X		580
MC710F	2	580	MC1314G		591	U5B991129X		581
MC711G		581	MC1550G		590	U5B991421X		584
MC711F	2	581	MC1554G		593	U5B991422X		584
MC714G		584	PA713		590	U5B991429X		584
MC714F	2	584	PA7601		590	U5B992329X	4	572
MC717P	3	570	PL990029	4	571	U5B992329X	3	583
MC724P		570	PL991021	1	580	U5F991121X	2	581
MC776P	3	572	PL991029		580	U5D770339X		590
MC781G		582	PL991129		581	U5D990029X	4	571
MC782G		583	PL991429		584	U5D990029X	3	582
MC790P		572	PL992329	4	572	μL900	4	571
MC799P		571	PL992329	3	583	μL911	3	581
MC810G		580	SN17810L	1	580	μL914	(4)	584 (570)
MC810F	2	580	SN17910L	1	580	μL923	4	572

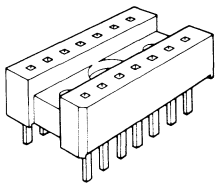
Note 1: Temperature range is narrower.
Note 2: Case Difference
Note 3: Milliwatt vs Medium power may require slight circuit value variations to optimize performance.
Note 4: Plastic replaces 2 metal units. (Case Difference)

IC MOUNTING SOCKETS

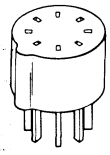
HEP451 (Pkg. of 2)
10-Pin IC Socket



HEP453
14-Pin Dual Inline IC Socket



HEP454 (Pkg. of 2)
8-Pin IC Socket



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